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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/004,614	11/01/2001	Yuan-sheng Huang	67,200-565	8180

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EXAMINER	
ALEJANDRO MULERO, LUZ L	
ART UNIT	**PAPER NUMBER**
1763	

DATE MAILED: 02/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/004,614	HUANG ET AL.	
	Examiner	Art Unit	
	Luz L. Alejandro	1763	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5,7-13 and 15-20* is/are pending in the application.

4a) Of the above claim(s) *20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-5, 7-13, 15-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 3-5, 7-8, 11-13, 15-17, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii et al., U.S. Patent 5,571,366 in view of Somekh et al., U.S. Patent 5,643,366 or Brors et al., EP 0276061.

Ishii et al. shows the invention as claimed including a semiconductor dry etching system comprising: a plasma chamber 2 in which reaction gases are introduced and reaction product particles formed fall down due to gravity (see col. 11, lines 37-39); an electrically biased mechanism (chuck 12') to hold a semiconductor wafer in the top of

the chamber (upside-down), thereby preventing particles from falling onto the wafer (see fig. 12 and col. 11, lines 23-40). With respect to the introduction of a polymer into the chamber, limitation is directed to a method limitation instead of an apparatus limitation. The method limitations are viewed as intended uses which do not further limit, and therefore do not patentably distinguish the claimed invention. The apparatus of Ishii et al. is capable of introducing gases that will produce a polymer as a reaction product.

Additionally, note that the apparatus of Ishii et al. further comprises: a) a vertically movable wafer lifter 76 to hold the wafer which comprises a tubular body having a substantially open-ended cap at a downward-facing end thereof against which the wafer is held, b) a bias supply 14 to the electrically biased mechanism, c) one or more coils coupled to a power supply, and d) a dielectric window as the lower wall of the chamber.

Ishii et al. does not expressly disclose that the wafer lifter is positioned at the top of the plasma chamber, has sidewalls defining a first diameter greater than the diameter of the wafer and a bottom having a hole therein having a second diameter less than the first diameter and less than the diameter of the wafer, the wafer exposed from the bottom of the wafer lifter through the hole therein, or wherein the wafer rests on an inner top surface of the bottom of the wafer lifter that is completely parallel as a whole to an outer bottom surface of the bottom of the wafer lifter, the inner top surface and the outer bottom surface of the bottom of the wafer lifter both completely perpendicular as a whole to the sidewalls of the wafer lifter defining the first diameter greater than the

second diameter. Somekh et al. discloses an apparatus which holds a workpiece 40 at the top of the chamber and a wafer lifter 76/125 being positioned at the top of the chamber, having sidewalls defining a first diameter greater than the diameter of the wafer and a bottom having a hole therein having a second diameter less than the first diameter and less than the diameter of the wafer, and wherein the wafer is exposed from the bottom of the wafer lifter through the hole therein (see, for example, figs. 3a-3f and their descriptions). Furthermore, note that in Somekh et al. the wafer rests on an inner top surface of the bottom of the wafer lifter that extends completely parallel as a whole to an outer bottom surface of the bottom of the wafer lifter, the inner top surface and the outer bottom surface of the bottom of the wafer lifter both extending completely perpendicular to the sidewalls of the wafer lifter as a whole and defining the first diameter greater than the second diameter. Additionally, Brors et al. discloses an apparatus which holds a workpiece 232 at the top of the chamber and a wafer lifter 234 being positioned at the top of the chamber, having sidewalls defining a first diameter greater than the diameter of the wafer and a bottom having a hole therein having a second diameter less than the first diameter and less than the diameter of the wafer, and wherein the wafer is exposed from the bottom of the wafer lifter through the hole therein (see, for example, fig. 14 and its description). Furthermore, in Brors et al. the wafer rests on an inner top surface of the bottom of the wafer lifter that is completely parallel as a whole to an outer bottom surface of the bottom of the wafer lifter, the inner top surface and the outer bottom surface of the bottom of the wafer lifter both completely perpendicular as a whole to the sidewalls of the wafer lifter defining the first

diameter greater than the second diameter. Therefore, in view of these disclosures, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the apparatus of Ishii et al. as to comprise the claimed wafer lifter because such a wafer lifter structure is a suitable alternative means for holding the wafer at the top of the chamber.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii et al. in view of Somekh et al., U.S. Patent 5,643,366 or Brors et al., EP 0276061, as applied to claims 1, 3-5, 7-8, 11-13, 15-17, and 19 above and further in view of Uchida, U.S. Patent 5,804,027 or Ishii et al., U.S. Patent 5,795,429.

Ishii et al. '366, Somekh et al. and Brors et al. are applied as above but do not expressly disclose that the one or more coils comprise one or more electromagnetic coils coupled to an electromagnetic supply. Uchida discloses an apparatus in which electromagnetic coils 6-8 connected to respective power sources are used to generate electromagnetic fields (see, for example, fig. 3). Similarly, Ishii et al. '429 discloses an apparatus in which electromagnetic coil 106 is excited by power supply 107 to form an electromagnetic field (see, for example, fig. 22). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the apparatus of Ishii et al. '366 modified by Somekh et al. or Brors et al., as to comprise one or more electromagnetic coils coupled to an electromagnetic supply since such structure is known and used in the art in order to generate electromagnetic fields.

Claims 10 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii et al., U.S. Patent 5,571,366 in view of Somekh et al., U.S. Patent 5,643,366 or Brors et al., EP 0276061, as applied to claims 1, 3-5, 7-8, 11-13, 15-17, and 19 above, and further in view of the Admitted Prior Art (APA).

Ishii et al., Somekh et al. and Brors et al., are applied as above but do not expressly disclose that the apparatus further comprises one or more multi-pole magnets. The APA shows a semiconductor etching system, comprising: a plasma chamber 202 in which a polymer is introduced, excess polymer forming and subsequently peeling off the inner walls of the chamber and falls down due to gravity; and an electrically biased mechanism comprising a wafer chuck 218 to hold the semiconductor wafer and a bias supply 222 to electrically bias the wafer chuck; one or more coils 210 connected to RF power 214; one or more multi-pole magnets 204/206 to cooperating with the coil to assist inducement of the varying magnetic field within the chamber; and a dielectric window 208 (see fig. 2 and paragraphs 002-0010 of the instant application, especially paragraphs 009-0010). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the apparatus of Ishii et al. modified by Somekh et al. or Brors et al., as to further comprise one or more multi-pole magnets as taught by the APA in order to assist in the generation of the varying magnetic field within the chamber.

Claims 1, 3-5, 7-8, 10-13, and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art (APA) in view of Ishii et al., U.S. Patent 5,571,366 and Somekh et al., U.S. Patent 5,643,366 or Brors et al., EP 0276061.

The APA shows the invention substantially as claimed including a semiconductor etching system, comprising: a plasma chamber 202 in which a polymer is introduced, excess polymer forming and subsequently peeling off the inner walls of the chamber and falls down due to gravity; and an electrically biased mechanism comprising a wafer chuck 218 to hold the semiconductor wafer and a bias supply 222 to electrically bias the wafer chuck; one or more coils 210 connected to RF power 214; one or more multi-pole magnets 204/206; and a dielectric window 208 (see fig. 2 and paragraphs 002-0010 of the instant application, especially paragraphs 009-0010).

APA does not expressly disclose an electrically biased mechanism and wafer lifter that hold the wafer upside-down within the plasma chamber. Ishii et al. discloses a semiconductor dry etching system comprising: a plasma chamber 2 in which reaction gases are introduced and reaction product particles formed fall down due to gravity (see col. 11, lines 37-39); an electrically biased mechanism (chuck 12') to hold a semiconductor wafer in the top of the chamber (upside-down), thereby preventing particles from falling onto the wafer; and a vertically movable wafer lifter 76 to hold the wafer (see fig. 12 and col. 11, lines 23-40). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the apparatus of the APA as to be arranged to be a face-down type apparatus comprising the electrically biased mechanism and wafer lifter that hold the wafer upside-down

within the plasma chamber as taught by Ishii et al., because in such a way the wafer to be processed can be protected from being contaminated by particles and the like, therefore further improving the yield and the throughput.

APA and Ishii et al. do not expressly disclose that the wafer lifter is positioned at the top of the plasma chamber, has sidewalls defining a first diameter greater than the diameter of the wafer and a bottom having a hole therein having a second diameter less than the first diameter and less than the diameter of the wafer, the wafer exposed from the bottom of the wafer lifter through the hole therein, or wherein the wafer rests on an inner top surface of the bottom of the wafer lifter that is completely parallel as a whole to an outer bottom surface of the bottom of the wafer lifter, the inner top surface and the outer bottom surface of the bottom of the wafer lifter both completely perpendicular as a whole to the sidewalls of the wafer lifter defining the first diameter greater than the second diameter. Somekh et al. discloses an apparatus which holds a workpiece 40 at the top of the chamber and a wafer lifter 76/125 being positioned at the top of the chamber, having sidewalls defining a first diameter greater than the diameter of the wafer and a bottom having a hole therein having a second diameter less than the first diameter and less than the diameter of the wafer, and wherein the wafer is exposed from the bottom of the wafer lifter through the hole therein (see, for example, figs. 3a-3f and their descriptions). Furthermore, note that in Somekh et al. the wafer rests on an inner top surface of the bottom of the wafer lifter that is completely parallel as a whole to an outer bottom surface of the bottom of the wafer lifter, the inner top surface and the outer bottom surface of the bottom of the wafer lifter both completely perpendicular as a

whole to the sidewalls of the wafer lifter defining the first diameter greater than the second diameter. Alternatively, Brors et al. discloses an apparatus which holds a workpiece 232 at the top of the chamber and a wafer lifter 234 being positioned at the top of the chamber, having sidewalls defining a first diameter greater than the diameter of the wafer and a bottom having a hole therein having a second diameter less than the first diameter and less than the diameter of the wafer, and wherein the wafer is exposed from the bottom of the wafer lifter through the hole therein (see, for example, fig. 14 and its description). Furthermore, note that in Brors et al. et al. the wafer rests on an inner top surface of the bottom of the wafer lifter that is completely parallel as a whole to an outer bottom surface of the bottom of the wafer lifter, the inner top surface and the outer bottom surface of the bottom of the wafer lifter both completely perpendicular as a whole to the sidewalls of the wafer lifter defining the first diameter greater than the second diameter. Therefore, in view of these disclosures, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the apparatus of the APA modified by Ishii et al. as to comprise the claimed wafer lifter because such a wafer lifter structure is a suitable alternative means for holding the wafer at the top of the chamber.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art (APA) in view of Ishii et al., U.S. Patent 5,571,366, and Somekh et al., U.S. Patent 5,643,366 or Brors et al., EP 0276061, as applied to claims 1, 3-5, 7-8,

10-13, 15-19 above, and further in view of Uchida, U.S. Patent 5,804,027 or Ishii et al., U.S. Patent 5,795,429.

APA, Ishii et al. '366, Somekh et al., and Brors et al. are applied as above but do not expressly disclose that the one or more coils comprise one or more electromagnetic coils coupled to an electromagnetic supply. Uchida discloses an apparatus in which electromagnetic coils 6-8 connected to respective power sources are used to generate electromagnetic fields (see, for example, fig. 3). Similarly, Ishii et al. '429 discloses an apparatus in which electromagnetic coil 106 is excited by power supply 107 to form an electromagnetic field (see, for example, fig. 22). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the apparatus of APA modified by Ishii et al. '366, Somekh et al., and Brors et al. as to comprise one or more electromagnetic coils coupled to an electromagnetic supply since such structure is known and used in the art in order to generate electromagnetic fields.

Response to Arguments

Applicant's arguments filed 12/02/04 have been fully considered but they are not persuasive.

With respect to the Somekh et al. reference, note that in Somekh et al., the inner top surface on which the wafer 139 rests extends completely parallel as a whole to the outer bottom surface of the wafer lifter. Furthermore, note that the portion of the inner and outer surfaces of the wafer lifter that the wafer either rests on or immediately

overlies are completely parallel with each other and completely perpendicular to the sidewalls of the wafer lifter.

Concerning the Brors reference, note that the portion of the inner and outer surfaces of the wafer lifter that the wafer either rests on or immediately overlies are completely parallel with each other and completely perpendicular to the sidewalls of the wafer lifter.

Notwithstanding the fact that the limitations regarding the configuration of the wafer lifter reads on the references as mentioned above, a prima facie case of obviousness still exists because no unexpected results have been shown with respect to the inner top surface of the wafer lifter which the wafer rests upon being completely parallel as a whole to an outer bottom surface of the wafer lifter and both the mentioned inner and outer surfaces of the wafer lifter being completely perpendicular as a whole to the sidewalls of the wafer lifter.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luz L. Alejandro whose telephone number is 571-272-1430. The examiner can normally be reached on Monday to Thursday from 7:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gregory L. Mills can be reached on 571-272-1439. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Luz L. Alejandro
Primary Examiner
Art Unit 1763

February 10, 2005